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EXAMINER	
GILES, NICHOLAS G	

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/782,862	KIM ET AL.	
	Examiner	Art Unit	
	NICHOLAS G. GILES	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-28* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims **1, 18, and 21** have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims **1-4, 6-8, 10, 13, 14, 17, 18, 21-23, and 25-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (U.S. Patent No. 7,102,677) in view of Conrads et al. (U.S. Patent No. 5,184,018).

Regarding claim **1**, Watanabe discloses:

> An image sensor, comprising: a plurality of row lines (pixel selection clock line 15 Fig. 7, 1:41-45); a plurality of column lines crossing the plurality of row lines (column line 16 Fig. 7, 1:46-48); a plurality of pixels (photodiode 1 Fig. 7, 1:32-35), each pixel formed at a respective crossing of one of the plurality of row lines with one of the plurality of column lines, each pixel generating a charge based on light incident thereon and selectively transferring the charge to the respective column line based on a single signal, the single signal being received from the respective row line (2:60-64); and a plurality of column driver circuits (driving transistor 31 and horizontal selection switching transistor 32 Fig. 7, 1:46-55), each

column driver circuit associated with one of the column lines and configured to generate an output voltage based on the charge on the associated column line (1:28-1:59, Fig. 7).

Watanabe is silent with regards to transferring the charge to the column line based on a single signal without receiving additional control signals. Conrads et al. discloses this in 5:57-6:35 and Fig. 1 where the row transistor 3 transfers the pixel signal to the row lines 8, 9, 10 based on a single signal. As can be seen in 6:28-35 this is advantageous in that only one amplifier is needed for each column. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include transferring the charge to the column line based on a single signal without receiving additional control signals.

Regarding claim **2**, see the rejection of claim 1 and note that Watanabe further discloses:

Each pixel comprises: a photoelectric transformation element converting incident light into a charge (Photodiode 1 Fig. 7); and a transfer circuit configured to transfer the charge to the respective column line based on the signal, the single signal being received from the respective row line (Pixel selection transistor 5 Fig. 7 1:41-45).

Regarding claim **3**, see the rejection of claim 2 and note that Watanabe further discloses:

Photoelectric transformation element includes a photo diode (Photodiode 1 Fig. 7).

Regarding claim **4**, see the rejection of claim 2 and note that Watanabe further discloses:

> Transfer circuit is a transistor connected between the photoelectric transformation element and the respective column line and having a gate connected to the respective row line (Pixel selection transistor 5 Fig. 7 1:41-45).

Regarding claim **6**, see the rejection of claim 1 and note that Watanabe further discloses:

> Each column driver circuit comprises: a driver circuit configured to generate a voltage based on the charge on the respective column line (driving transistor 31, Fig. 7, 1:28-1:59); and an active load connected between an output of the driver circuit and ground (load transistor 33 Fig. 7, 1:55-59).

Regarding claim **7**, see the rejection of claim 6 and note that Watanabe further discloses:

> Driver circuit includes a drive transistor having a first electrode, second electrode and a gate, the first electrode being connected to a supply voltage, the second electrode serving as an output of the column driver circuit and connected to the active load, and the gate controlling operation of the drive transistor based on the charge on the associated column line (driving transistor 31, Fig. 7, 1:28-1:59).

Regarding claim **8**, see the rejection of claim 7 and note that Watanabe further discloses:

> Active load includes a load transistor connected between the drive transistor and ground (load transistor 33 Fig. 7, 1:55-59).

Regarding claim **10**, see the rejection of claim 6 and note that Watanabe further discloses:

> Driver circuit generates a reference voltage when a reset circuit resets the charge of each pixel associated with the associated column line (2:35-50).

Regarding claim **13**, see the rejection of claim 6 and note that Watanabe further discloses:

> Column driver circuit further comprises: a start circuit configured to selectively output the generated voltage as an output of the column driver circuit (horizontal selection switching transistor 32 Fig. 7, 1:46-55).

Regarding claim **14**, see the rejection of claim 13 and note that Watanabe further discloses:

> Driver circuit includes a drive transistor having a first electrode, second electrode and a gate, the first electrode being connected to a supply voltage, the second electrode connected to the start circuit, and the gate controlling operation of the drive transistor based on the charge on the associated column line (driving transistor 31, Fig. 7, 1:28-1:59); the start circuit includes a start transistor connected between the drive

transistor and the active load with output of the start transistor to the active load serving as output of the column driver circuit (horizontal selection switching transistor 32 Fig. 7, 1:46-55); and the active load includes a load transistor connected between the start transistor and ground (load transistor 33 Fig. 7, 1:55-59).

Regarding claim **17**, see the rejection of claim 1 and note that Watanabe further discloses:

One column driver circuit is associated with each of the column lines.

Regarding claim **18**, Watanabe discloses:

An image sensor, comprising: a plurality of row lines (pixel selection clock line 15 Fig. 7, 1:41-45); a plurality of column lines crossing the plurality of row lines (column line 16 Fig. 7, 1:46-48); a plurality of pixels, each pixel formed at a respective crossing of one of the plurality of row lines with one of the plurality of column lines, each pixel generating a charge based on light incident thereon and selectively transferring the charge to the respective column line based on a single signal, the single signal being received from the respective row line (photodiode 1 Fig. 7, 1:32-35); and a plurality reset circuits, one reset circuit being associated with each of the column lines and configured to reset the charge of each pixel associated with the associated column line (reset gate transistor 3 Fig. 7, 1:32-35).

Watanabe is silent with regards to transferring the charge to the column line based on a single signal without receiving additional control signals. Conrads et al. discloses this in 5:57-6:35 and Fig. 1 where the row transistor 3 transfers the pixel signal to the row lines 8, 9, 10 based on a single signal. As can be seen in 6:28-35 this is advantageous in that only one amplifier is needed for each column. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include transferring the charge to the column line based on a single signal without receiving additional control signals.

Regarding claim **21**, Watanabe discloses:

> An image sensing method, comprising: selectively applying a plurality of voltages to a plurality of column lines of an image sensor based on a single signal, the single signal being received from each or a plurality of row lines, the plurality of voltages based on charges generated by a plurality of pixels of the image sensor (1:28-1:59, Fig. 7); and generating, for each column line, a data voltage as an output voltage based on the applied voltage (using driving transistor 31 and horizontal selection switching transistor 32, 1:28-1:59, Fig. 7).

Watanabe is silent with regards to transferring the charge to the column line based on a single signal without receiving additional control signals. Conrads et al. discloses this in 5:57-6:35 and Fig. 1 where the row transistor 3 transfers the pixel signal to the row lines 8, 9, 10 based on a single signal. As can be seen in 6:28-35 this is advantageous in that only one amplifier is needed for each column. For this reason it

would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include transferring the charge to the column line based on a single signal without receiving additional control signals.

Regarding claim **22**, see the rejection of claim 21 and note that Watanabe further discloses:

> Prior to the applying step, comprising: resetting the charge of each pixel (2:35-50).

Regarding claim **23**, see the rejection of claim 22 and note that Watanabe further discloses:

> Resetting step simultaneously resets the charge of each pixel (2:35-50 and Fig. 8).

Regarding claim **25**, see the rejection of claim 22 and note that Watanabe further discloses:

> Generating a reference voltage as the output voltage after the resetting step (2:35-50).

Regarding claim **26**, see the rejection of claim 25 and note that Watanabe further discloses:

> Generating a reference voltage step generates the reference voltage until the applying step (2:35-50 and Fig. 8).

Regarding claim **27**, see the rejection of claim 22 and note that Watanabe further discloses:

Repeating the resetting, applying and generating steps for each row of pixels in the image sensor (Fig. 8).

Regarding claim **28**, see the rejection of claim 22 and note that Watanabe further discloses:

Initializing the output voltage (2:35-50).

3. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Conrads et al. in further view of Yang et al. (U.S. Patent No. 6,180,969).

Regarding claim **5**, see the rejection of claim 4 and note that Watanabe is silent with regards to using depletion mode NMOS transistors. Yang discloses this in 4:37-40. Yang discloses in 4:37-40 that an advantage to this is that the charge transfer efficiency is improved and they reduce voltage drop and/or loss of signal charge. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include using depletion mode NMOS transistors.

4. Claims **9, 11, 16, 19, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Conrads et al. in further view of Prater (U.S. Patent No. 5,654,537).

Regarding claim **9**, see the rejection of claim 6 and note that Watanabe is silent with regards to a reset circuit resetting the charge of each pixel associated with a column line. Prater discloses this in 3:60-4:5. Prater discloses in 3:62-4:5 that an

advantage to using this is that any voltage between V.sub.DD and ground can be applied to the column line and reset FET 54. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include a reset circuit resetting the charge of each pixel associated with a column line.

Regarding claim **11**, see the rejection of claim 9 and note that Prater further discloses:

> Reset circuit includes a transistor connected between a supply voltage and the associated column line (3:60-4:5).

Prater discloses in 3:60-4:5 that an advantage to this is that the use of the reset transistors allows any voltage between V.sub.DD and ground to be applied to the column line and reset FET 54. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include a reset transistor connected between a supply voltage and the column line.

Regarding claim **16**, see the rejection of claim 1 and note that Watanabe is silent with regards to the driver circuit resetting the charge of each pixel associated with the column line. Prater discloses this in 3:60-4:5. Prater discloses in 3:62-4:5 that an advantage to using this is that any voltage between V.sub.DD and ground can be applied to the column line and reset FET 54. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include a reset circuit resetting the charge of each pixel associated with a column line.

Regarding claim **19**, see the rejection of claim 18 and note that Watanabe is silent with regards to a reset transistor connected between a supply voltage and the column line.

> Reset circuit includes a transistor connected between a supply voltage and the associated column line (3:60-4:5).

Prater discloses in 3:60-4:5 that an advantage to this is that the use of the reset transistors allows any voltage between V.sub.DD and ground to be applied to the column line and reset FET 54. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include a reset transistor connected between a supply voltage and the column line.

Regarding claim **24**, see the rejection of claim 22 and note that Watanabe is silent with regards to applying a supply voltage to each column line to reset the pixel. Prater discloses:

> Resetting step includes applying a supply voltage to each column line to reset the charge of each pixel (3:60-4:5).

Prater discloses in 3:62-4:5 that an advantage to using this is that any voltage between V.sub.DD and ground can be applied to the column line and reset FET 54. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include a reset circuit resetting the charge of each pixel associated with a column line.

5. Claims **12 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Conrads et al. in further view of Prater in further view of Yang et al. (U.S. Patent No. 6,180,969).

Regarding claim **12**, see the rejection of claim 19 and note that Watanabe and Prater are silent with regards to using depletion mode NMOS transistors. Yang discloses this in 4:37-40. Yang discloses in 4:37-40 that an advantage to this is that the charge transfer efficiency is improved and they reduce voltage drop and/or loss of signal charge. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include using depletion mode NMOS transistors.

Regarding claim **20**, see the rejection of claim 19 and note that Watanabe and Prater are silent with regards to using depletion mode NMOS transistors. Yang discloses this in 4:37-40. Yang discloses in 4:37-40 that an advantage to this is that the charge transfer efficiency is improved and they reduce voltage drop and/or loss of signal charge. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Watanabe include using depletion mode NMOS transistors.

Allowable Subject Matter

6. Claim **15** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim **15**, no prior art could be located that teaches or fairly suggests the start transistor being an enhancement mode transistor and being larger than the drive transistor and load transistor in combination with the rest of the limitations of the claim.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NICHOLAS G. GILES whose telephone number is

(571)272-2824. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nicholas G Giles/
Examiner, Art Unit 2622

/Sinh N Tran/
Supervisory Patent Examiner, Art Unit 2622